## 1.1 MIPI CSI System

## 1.1.1 MIPI CSI introduction

CSI2 (Camera Serial Interface2) defines protocols between a peripheral device (camera) and a host processor. It provides a cost efficient solution for mobile device. MIPI CSI System integrates the function of CSI2 TX and RX. RX receives image data from MIPI CSI sensor and TX sends the processed image data out to display.

## 1.1.2 Architecture



Figure: MIPI CSI System Architecture

The MIPI CSI System consists of four blocks:

DPHY: the physical layer of MIPI CSI and DSI.

INTERCONNECT: the control logic of data exchange between transmitter or receiver and DPHY.

TWO\_LANE\_RX: two lane controller of CSI receiver.

FOUR\_LANE\_RX: four lane controller of CSI receiver.

FOUR\_LANE\_TX: four lane controller of CSI transmitter.

## 1.1.3 Feathers

* 1.5Gbps per lane in HS mode, up to 6Gbps in one four lane link.
* In RX mode, support up to 4 4lane link or 8 2\_lane link.
* In TX mode, support one 4lane (can configured as 1~4 lane) link.
* Follow data type can be supported in TX mode.
* RGB888
* YUV420 8-bit (legacy) / 8-bit / 10-bit
* YUV422 8-bit / 10-bit
* YUV444 8-bit / 10-bit
* Follow data type can be supported in RX mode.
* YUV420 8-bit (legacy) / 8-bit / 10-bit / 8-bit (CSPS) / 10-bit (CSPS)
* YUV422 8-bit / 10-bit
* RGB888 / RGB666 / RGB565 / RGB555 / RGB444
* RAW6 / RAW7 / RAW8 / RAW10 / RAW12 / RAW14 / RAW16
* User define data type